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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/010,525	12/06/2001	Robert S. Chau	042390.P4222D3	1842
7.	590 01/11/2006	EXAM	EXAMINER	
Michael A. Bo		LOKE, STEV	LOKE, STEVEN HO YIN	
BLAKELY, SO	OKOLOFF, TAYLOR &			
Seventh Floor		ART UNIT	PAPER NUMBER	
12400 Wilshire		2811		
Los Angeles, CA 90025-1030			DATE MAILED: 01/11/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	10/010,525	CHAU ET AL.				
Office Action Summary	Examiner	Art Unit				
	Steven Loke	2811				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
<ul> <li>A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.</li> <li>Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.</li> <li>If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.</li> <li>Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).</li> </ul>						
Status						
1) Responsive to communication(s) filed on 27 Ap	oril 2005					
·= ·	action is non-final.					
<u>,                                     </u>						
closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>30,32,36 and 37</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>30, 32, 36, 37</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9) The specification is objected to by the Examiner.						
10) The drawing(s) filed on is/are: a) □ accepted or b) □ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)	A) T Intonian Comment	/PTO-413)				
1)  Notice of References Cited (PTO-892) 2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)	4)	ate				
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	5) Notice of Informal P 6) Other:	atent Application (PTO-152)				

1. Claims 30, 32, 36 and 37 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification never discloses depositing a metal layer over the sidewall spacers and the gate electrode to a thickness over the gate electrode sufficient to form a silicide having a height less than the spacer height when a semiconductor material film on the gate electrode and on the source/drain regions as claimed in claim 30.

2. Claims 30, 32, 36 and 37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 30, line 12, the phrase "a silicide layer" is unclear whether it is being referred to the silicide in line 11 of claim 30.

Claim 30, lines 13-14, the phrase "the third thickness less than the spacer height" is unclear as to what element in the semiconductor device has the third thickness. It is also unclear where are the first and second thicknesses in the semiconductor device.

Claim 37, lines 1-2, the phrase "the sidewall spacers are less than 300Å in width" is unclear whether each of the sidewall spacers has a width less than 300Å or the total width of the two sidewall spacers is less than 300Å.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 30, 36 and 37 insofar, as in compliance with 35 USC 112, are rejected 4. under 35 U.S.C. 102(b) as being clearly anticipated by Deleonibus (U. S. Patent no. 5,314,832).

In regards to claim 30, Deleonibus shows all the elements of the claimed invention in figs. 1A-1H. It discloses a method of forming a semiconductor device, comprising: forming a gate electrode [8a] on a gate dielectric layer [6] formed on a substrate [2]; forming a pair of source/drain regions [32, 34] on opposite sides of the gate electrode; forming a semiconductor material film [28] on the gate electrode [8a] and on the source/drain regions [32, 34]; forming a pair of sidewall spacers [24, 26] on opposite sides of the gate electrode [8a] and the gate dielectric layer [6], the sidewall spacers having a spacer height; depositing a metal layer (Since the silicide layers [29] are formed on the source, drain and gate by the self-aligned process using transition metal, it is inherent that a metal layer is formed on the gate, source and drain layers [28] and the sidewall spacers [24] because the self-aligned process only used a layer of metal to form the silicide layers.) over the sidewall spacers [24] and the gate electrode [8a, 28] to a thickness over the gate electrode sufficient to form a silicide [29] having a height less than the spacer height [24]; forming a silicide layer [29] on the semiconductor material film [28], the thickness of the silicide layer [29] is less than the spacer height and the spacers inherently confine the silicide to prevent silicide encroachment because the spacers block the connection between the gate silicide and the source/drain silicides.

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In regards to claim 36, Deleonibus further discloses the gate electrode [8a] comprises polysilicon.

In regards to claim 37, Deleonibus further discloses each of the sidewall spacers [26] is less than 300Å in width (col. 8, lines 43-47).

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Deleonibus.

In regards to claim 32, Deleonibus differs from the claimed invention by not showing the sidewall spacers comprise silicon nitride.

It would have been obvious for the sidewall spacers comprise silicon nitride, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

It would have been obvious for the sidewall spacers comprise silicon nitride because it depends on the desired capacitances between the gate and source regions and between the gate and drain regions.

- 7. Applicant's arguments with respect to claims 30, 32, 36 and 37 have been considered but are moot in view of the new ground(s) of rejection.
- 8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl January 8, 2006 Stever Sole